REMARKS

Claims 1-5 are pending in this application, of which claim 1 has been amended. No new claims have been added.

Claims 1-3 and 5 stand rejected under 35 USC §103(a) as unpatentable over **Ueda et al.** in view of **Nakata et al.** (both previously applied).

Applicants respectfully traverse this rejection.

As noted in Applicants' response of May 27, 2003, **Ueda et al.** discloses a flip-flop circuit constituted by two latch circuits of the same structure that are cascaded. Each latch circuit includes an inverter formed of a P channel transistor and an N channel transistor, an N channel transistor connected between a common node and a ground node, and two data input/output terminals. Two kinds of clock signals supplied to gates of N channel transistors are complementary to each other.

The Examiner has admitted that **Ueda et al.** does not disclose that a charge recycle power source is used to generate the clock signal, but has cited **Nakata et al.** for teaching this feature.

Applicants respectfully disagree. Although Fig.1 (b) of **Nakata et al.** shows non-rectangular power clock waveforms, as in the present invention, neither **Ueda et al.** nor **Nakata et al.** teaches, mentions or suggests satisfaction of the following inequality recited in claim 1 of the instant application:

$$|V_{TN}|+|V_{TP}| \geq VDD,$$

where V_{TN} is a threshold of the n-channel MOSFET transistor, V_{TP} is a threshold of the

p-channel MOSFET, and VDD is an output voltage of the charge recycle power source.

Nakata et al. is directed to a charge recycle power source. The present invention further improves a charge recycle power source, by introducing the inequality recited in claim 1.

A charge recycle power source reduces power consumption to 1/10 as compared with that of the prior art (discussed on page 7, lines 21-23 of the specification). However, because a waveform of a charge recycle power source has a transient period when a wave form rises and falls gradually, a short-circuit current flows from a power source to ground during the transient period. No prior art reference discusses the short-circuit current in a transient period in a charge recycle power source.

The present invention solves the problem of a short-circuit current by introducing the inequality, and this is discussed in detail on pages 8 and 9 of the specification.

The Examiner has urged that the satisfaction of this inequality is inherent because the combination of the prior art creates the same structure as claimed. The Examiner has also urged that values used for VDD and the transistor thresholds are seen as design expedients dependent on the particular environment and the desired outcome.

Applicants respectfully disagree. The inequality pertains to the register circuit, not the clock circuit. Furthermore, the criticality of this feature to the patentability of the present invention is noted on page 9, lines 19-21 of the specification, which discloses that the satisfaction of this inequality "allows no short-circuit current from a power source to ground of a logic gate

in a D-latch circuit 10." This advantage is not present in the prior art and is not mentioned or suggested in either **Ueda et al.** or **Nakata et al**.

It should be noted that in conventional design of a transistor logic circuit, threshold voltages $|V_{TN}|$ and $|V_{TP}|$ are each selected to be about 20% of a power source voltage VDD. For instance, when VDD is 5 volts, threshold voltages $|V_{TN}|$ and $|V_{TP}|$ would each be around 1 volt. This does not satisfy the inequality.

Thus, the Examiner's contention that such inequality is inherent in the combination of the applied prior art references is not well-taken, and the 35 USC §103(a) rejection should be withdrawn.

The Examiner has indicated that claim 4 would be allowed if rewritten in independent form. Applicants respectfully defer this action until a FINAL Office Action, if any, is received.

In view of the aforementioned amendments and accompanying remarks, claims 1-5, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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